What is claimed is:

1. A method comprising determining whether a prefetched address is identical to a received address.

2. A method as defined in Claim 1, further comprising, if the prefetched address is not identical to the received address, interrupting data transfer from a memory and applying the received address to the memory.

3. A method as defined in Claim 2, wherein determining whether the prefetched address is identical to the received address comprises:

comparing the received address to the prefetched address using a comparator.

4. A method as defined in Claim 3, wherein the comparator is a gated comparator.

5. A method as defined in Claim 4, wherein the comparator is enabled by a signal that assumes a predetermined logic level when prefetching of a respective prefetched address has been accomplished.

6. A method as defined in Claim 3, wherein the comparator provides a first output when the prefetched address is determined to be identical to the received

address and a second output when the prefetched address is determined not to be identical to the received address.

7. A method as defined in Claim 6, further comprising:

coupling the received address to a first address input of a multiplexer, the multiplexer having an output to couple to the memory;

coupling the prefetched address to a second address input of the multiplexer;

selecting the prefetched address in response to the first output from the comparator; and

selecting the received address in response to a the second output from the comparator.

8. A method as defined in Claim 7, further comprising:

coupling the comparator output to the memory so that the data output of the memory is interrupted in response to the appearance of a the second output signal at the comparator output.

9. A method as defined in Claim 8, further comprising:

enabling the comparator upon the occurrence of a signal that indicates that valid prefetch address data exists upon completion of a prefetch operation.

10. An apparatus comprising:

an address multiplexer having a control input; and

an address comparator having a received address input, a prefetched address input, and an output coupled to the control input of the address multiplexer.

11. An apparatus as defined in Claim 10, wherein the address comparator output is coupled to assume a first value when the received address input is identical to the prefetched address input and to assume a second value when the received address input is not identical to the prefetched address input.

12. An apparatus as defined in Claim 11, wherein when the address comparator output is coupled to assume the first value, the address multiplexer is coupled to provide the prefetched address to the address multiplexer output.

13. An apparatus as defined in Claim 11, wherein when the address comparator output is coupled to assume the second value, the address multiplexer is coupled to provide the received address to the address multiplexer output.

14. An apparatus as defined in Claim 11, wherein the address comparator has an enable input to couple to a

signal that assumes a predetermined enabled value when valid prefetched address data exists so that the address comparator is enabled only when valid prefetched address data is determined to exist at the address comparator prefetch address input.

15. An apparatus as defined in Claim 14, wherein when the address comparator output is coupled to assume the first value, the multiplexer is coupled to provide the prefetched address to the multiplexer output.

16. An apparatus as defined in Claim 14, wherein when the address comparator output is coupled to assume the second value, the multiplexer is coupled to provide the received address to the multiplexer output.

17. An apparatus as defined in Claim 10, further comprising:

an address latch having a first input to accept a prefetched address, a second input to accept a received address, and a address output coupled to the received address input of the multiplexer to provide the received address to the multiplexer.

18. An apparatus as defined in Claim 17, wherein the address latch has an output coupled to an enable input of

the address comparator to cause the address comparator to be enabled when valid prefetched address data is determined to exist at the first input of the address latch.

19. An apparatus as defined in Claim 18, wherein the address multiplexer has a first address output coupled to the memory and a second address output coupled to the prefetched address input of the comparator.

20. An apparatus as defined in Claim 19, wherein the address comparator output assumes a first value when the received address input is identical to the prefetched address input and assumes a second value when the received address input is not identical to the prefetched address input.

21. A system comprising:

a dynamic prefetch circuit coupled to a memory, the dynamic prefetch circuit comprising:

an address multiplexer having a control input; and

an address comparator having a received address input, a prefetched address input, and an output coupled to the control input of the multiplexer; and

an antenna coupled to the dynamic prefetch circuit.

22. An system as defined in Claim 21, wherein the address comparator output is coupled to assume a first value when the received address input is identical to the prefetched address input and to assume a second value when the received address input is not identical to the prefetched address input.

23. A system as defined in Claim 22, wherein when the comparator is coupled to assume the first value, the multiplexer is coupled to provide the prefetched address to the multiplexer output.

24. A system as defined in Claim 21, wherein the dynamic prefetch circuit further comprises an address latch, wherein the address latch comprises:

a first address input to couple to a prefetched address generator;

a second address input to couple to a source of received addresses; and

an address output coupled to a received address input of the address multiplexer.

25. A system as defined in Claim 24, wherein the address latch further comprises:

a PFDONE input to receive a signal that indicates that valid prefetched address data exists at the first address input of the address latch;

an ADV input to receive a signal that indicates that valid received address data is present at the second address input of the address latch;

a CLK input coupled to a system clock; and

a PFVALID output coupled to an enable input of the comparator to cause the comparator to be enabled only when valid prefetched address data is determined to exist at the prefetched address input of the comparator and to cause the comparator output to change state synchronously with the system clock.

26. A system as defined in Claim 25, wherein the address multiplexer has an output coupled to the prefetched address input of the comparator.

27. An article comprising a machine-readable storage medium containing instructions that, if executed, enable a system to determine whether a prefetched address is identical to a received address.

28. An article as defined in Claim 27, further comprising instructions that, if executed, enable the system to apply a received address to a memory and to interrupt data transfer from the memory if the prefetched address is not identical to the received address.

29. An article as defined in Claim 28, further comprising instructions that, if executed, enable the system to compare the prefetched address and the received address when prefetching a respective prefetched address has been accomplished.

30. An article as defined in Claim 29, further comprising instructions that, if executed, enable the system to select an address to be applied to the memory synchronously with a system clock.